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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/212,657	12/15/98	MOON	D 8733D-6890

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EXAMINER	
VU,Q	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 04/24/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/212,657	MOON, DAE-GYU	
	Examiner	Art Unit	
	Quynh-Nhu H. Vu	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

1. Applicant's amendment filed on 1/30/01 has been received and entered in the case. The rejection of claims 1-18 is maintained. A new ground of rejection is introduced in view of the newly added claims 19-22.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claims 1 and 9, the phrase "formed using the region as the substrate" is not understood. The remaining claims are also rejected since they depend on the indefinite claims. In the below rejections, the above phrase is interpreted as "formed at the first (second, third) region of the substrate".

This rejection stands because Applicant did not provide any explanation regarding the meaning of the phrase "formed using the region as the substrate". Therefore, the intended scope of these claims is unclear because of the above-mentioned phrase.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 7 and 9-10 are rejected under 35 U.S.C. 102(b) as being unpatentable by Applicant's Prior Art.

Applicant 's Prior Art disclose in Figs. 1C and 2 a system-on-panel type liquid crystal display comprising: a substrate (100) including first, second and third region; a pixel array formed at the first region of the substrate; a driver (data driving circuit and gate driving circuit) formed at the second region of the substrate; and a control unit formed at the third region of the substrate. The switching devices formed of single crystal silicon are inherently included in the control unit. See specification, page 5, last paragraph; page 6.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3-6, 8, 11-18, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant 's Prior Art Figs. 1C and 2 in view of Funada et al. [PN 5,696,388].

Applicant's Prior Art Figs. 1C and 2, as applied in prior rejection, disclose all claimed subject matter except that the pixel array has an active layer formed of polycrystalline silicon, single crystalline silicon or amorphous silicon, and the driver has an active layer formed of amorphous silicon or single crystalline silicon.

Funada et al. disclose in column 1, lines 17- 68 that the thin film transistors (TFTs) which include the pixel array and driver are formed of amorphous silicon, single crystalline silicon, or polycrystalline silicon. Applicant's Prior Art Fig. 1B discloses that it is known to employ a driver having an active layer formed of polycrystalline silicon (specification, page 3, last paragraph; page 4, first paragraph).

Thus, it would have been obvious at the time the invention was made to a person having ordinary skill in the art in view of Funada et al. to employ amorphous silicon, single crystal silicon and polycrystalline for the following reasons: amorphous silicon is most generally used because it has low manufacturing temperature and can be relatively readily manufacturing by a gas phase method so as to being wealthy in productivity. However, the single crystalline silicon is has good electrical conductivity, as compared to amorphous silicon and polycrystalline silicon. Polycrystalline silicon is easily fabricated on glass substrate and has good electrical conductivity, as compared to amorphous silicon.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant 's Prior Art Figs. 1C and 2 in view of Applicant's Prior Art Fig. 1A.

Applicant 's Prior Art disclose in Figs. 1C and 2 a system-on-panel liquid crystal display comprising: a substrate including first, second and third regions; a pixel array formed on the substrate at the first region; a driver (data driving circuit and gate driving circuit) formed on the substrate at the second region, the driver having an active layer (TFTs) including polysilicon (3) (specification, page 4, line 26). However, source/drain region is belongs to active layer; and a control unit formed on the substrate at the third region. The switching devices formed of single crystal silicon are inherently included in the control unit (specification, page 5, last paragraph, and page 6). Applicant's Prior Art in Fig. 1C does not disclose an active layer including amorphous silicon.

However, Applicant's Prior Art Fig. 1A disclose an active layer (TFT or thin film transistor) including amorphous silicon (specification, page 3, line 9).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to employ the amorphous silicon TFT, as applicant's cited in Fig. 1A, for the benefit of achieving quick switching operations in an efficient manner.

8. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant 's Prior Art Figs. 1C and 2 in view of Funada et al. [US 5,696,388].

Applicant 's Prior Art disclose in Figs. 1C and 2 a system-on-panel liquid crystal display comprising: a substrate including first, second and third regions; a pixel array

formed on the substrate at the first region; a driver (data driving circuit and gate driving circuit) formed on the substrate at the second region, the driver having an active layer (TFTs) including polysilicon (3) (specification, page 4, line 26). However, source/drain region is belongs to active layer; and a control unit formed on the substrate at the third region. The switching devices formed of single crystal silicon are inherently included in the control unit (specification, page 5, last paragraph, and page 6). Applicant's Prior Art in Fig. 1C does not disclose an active layer formed of amorphous silicon, single crystalline silicon.

Funada et al. disclose the thin film transistors (TFTs) which include the pixel array having an active layer are formed of amorphous silicon, single crystalline silicon (col. 1, lines 17-68).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to employ the amorphous silicon, single crystalline silicon, as taught by Funada et al., for the following benefits: amorphous silicon having low manufacturing temperature and being relatively readily manufacturing by a gas phase method so as to being wealthy in productivity. However, the single crystalline silicon has good electrical conductivity.

Response to Arguments

9. Applicant's arguments filed 1/30/01 have been fully considered but they are not persuasive.

Applicant's arguments are as follows:

1) The cited reference does not teach or suggest at least these elements of the claimed invention. The supporting text for Figure 1C directly teaches mounting devices, such as a CPU and a controller, which were already formed on a silicon wafer by a separate semiconductor process, on a substrate, not forming them on the substrate.

2) The term "driver" is used to refer to a TFT, which drives a pixel. However, the drivers recited in the present specification with references to Fig. 1B are the driver ICs that are outside of the pixel array, not the TFTs within the pixel array.

Examiner's response to Applicant's argument is as follows:

Response the first argument:

First, figure 1C clearly shows the mounting devices such as a CPU and a controller being formed on a substrate 100.

Second, figure 2 clearly shows a CPU and a controller formed on a glass substrate 1 (specification, page 4, lines 24-25).

Third, in the last office action, examiner indicated that the phrase "formed using the region as the substrate" interpreted as "formed at the first (second, third) region on the substrate". The Applicant was agreed with the Examiner's interpretation on page 3, lines 3-6. So, Applicant's Prior Art Figs. 1c and 2 met all claim limitations to rejected claims 1-2, 7,9 and 10.

Fourth, the term "formed using" of claim 1 appears to be "product by process" limitation. Therefore, this limitation has not been given patentable weight. See MPEP § 2113.

Fifth, the limitation upon which applicant relies (i.e., mounting devices such as a CPU and a controller, which were already formed on a silicon wafer by a separate semiconductor process) are not recited in the rejected claim (s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

Response the second argument:

Again, the arguments that "the drivers recited in the present specification with references to Fig. 1B are the driver ICs that are outside of the pixel array, not the TFTs within the pixel array" are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations form the specification are not read into the claims. Furthermore, the applicant recited that the driver has an active layer formed of polycrystalline silicon (claims 4, 15 and 17), single crystalline silicon (claim 8 and 18). As one skill in the art know that any TFTs have an active layer. Furthermore, Funada et al. disclose that TFTs have the active layer which is formed of polycrystalline silicon or single crystalline silicon. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to employ the active layer formed of crystalline silicon semiconductor, i.e., polycrystalline silicon, single crystalline silicon, for the benefits of simplifying fabricating and good electrical conductivity.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quynh-Nhu H. Vu whose telephone number is 703-305-0850. The examiner can normally be reached on 7:30-5:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Sikes can be reached on 703-308-4842. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QNV
April 23, 2001

William L. Sikes
Supervisory Patent Examiner
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